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Doping technologies for InP membranes on silicon for nanolasers

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ABSTRACT

We present a systematic study of Zn thermal diffusion and Si ion implantation with subsequent rapid thermal annealing as the methods to fabricate lateral p-i-n junctions in InP membranes on silicon for use in electrically pumped in-plane nanolasers. We describe in detail optimized fabrication steps, which include MOVPE growth of InGaAs/InP epilayers, 2" InP to 4" SiO_2/Si direct bonding, and several cycles of DUV lithography. Values for sheet resistance of p-InGaAs/InP and n-InP membranes are obtained, which correspond to carrier concentration levels higher than 10^{18} cm^{-3} for both Zn-diffused p-InP and Si-implanted n-InP.

Keywords: InP membrane, Si ion implantation, Zn diffusion, doping, III-V on silicon, wafer bonding

1. INTRODUCTION

Nowadays on-chip electrical interconnects use more than a half of the total processer power consumption and the power fraction used for communication increases for each technology node. The power consumption can be significantly reduced if on-chip electrical links are replaced by the optical links[1]. To implement optical on-chip interconnects, a crucial component is an electrically driven nanolaser. A good candidate for that is photonic crystal (PhC) InP-based nanolaser. There are two different approaches to electrical injection: vertical injection[2] and lateral[3,4,5]. Following recent demonstrations[6], design with the lateral electrical injection is the most promising. In this work, we investigate and optimize Zn thermal diffusion in MOVPE reactor and Si ion implantation with subsequent rapid thermal annealing as the methods to fabricate lateral p-i-n junction in InP membrane. All processing is done on a silicon substrate to be compatible with silicon photonics fabrication infrastructure.

2. FABRICATION OVERVIEW

The fabrication process starts with 2" InP substrates, on which we grow epitaxial layers of lattice-matched $In_{0.53}Ga_{0.47}As$ (InGaAs) and InP by means of metal organic vapor phase epitaxy (MOVPE) (Fig. 1a). These layers are designed to have only intrinsic carrier concentration and are not intentionally doped. Then the 2" InP wafer is directly bonded to a 4" silicon wafer with 1.3 µm of thermally grown SiO_2 on top (Fig. 1b). The 4" Si wafer size is needed to be able to process sample with deep ultraviolet (DUV) lithography due to limitations of the DUV stepper.

Direct bonding includes the following steps. First, a thin (3 nm) layer of Al_2O_3 is deposited on both InP and Si wafers by atomic layer deposition (ALD). Second, wafers are gently pressed against each other at room temperature in order to be pre-bonded. Third, they are annealed at 300°C for 1 hour to increase the bond strength[7]. Al_2O_3 is chosen as an intermediate layer because it is characterized by large density of –OH groups[8], which attribute to high bonding strength.

Once bonded, the InP substrate is etched away by HCl. InGaAs and InP etch stop layers are etched by $1H_2SO_4$:$8H_2O_2$:$8H_2O$ and 1HCl:$4H_3PO_4$, respectively, leaving a membrane consisting of 50 nm InGaAs and 250 nm InP bonded to SiO_2/Si substrate (Fig. 1c). After alignment marks defining using DUV lithography and InGaAs/InP/SiO_2 dry etching, the next steps are Si ion implantation and Zn thermal diffusion (Fig. 1d). These steps are described in detail in the

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following sections. Then trenches in InGaAs/InP membrane are etched using reactive ion etching (RIE) with CH_4/H_2 chemistry (Fig. 1e). The role of trenches is to confine current in the designed areas. Next, InGaAs layer is wet etched everywhere except areas designed for "P" metal contacts (Fig. 1f). InGaAs is used as an intermediate layer between p-InP and "P" metal contacts due to poor performance of metal contacts directly to p-InP. Finally, "P" metal contacts (Ti\Pt\Au) (Fig. 1g) and "N" metal contacts (Ni\Ge\Au) (Fig. 1h) are fabricated on p-InGaAs/p-InP and n-InP, respectively, by using the lift-off technique. Sample is then rapid thermal annealed at 430°C to alloy n-contact and improve p-contact resistivity.

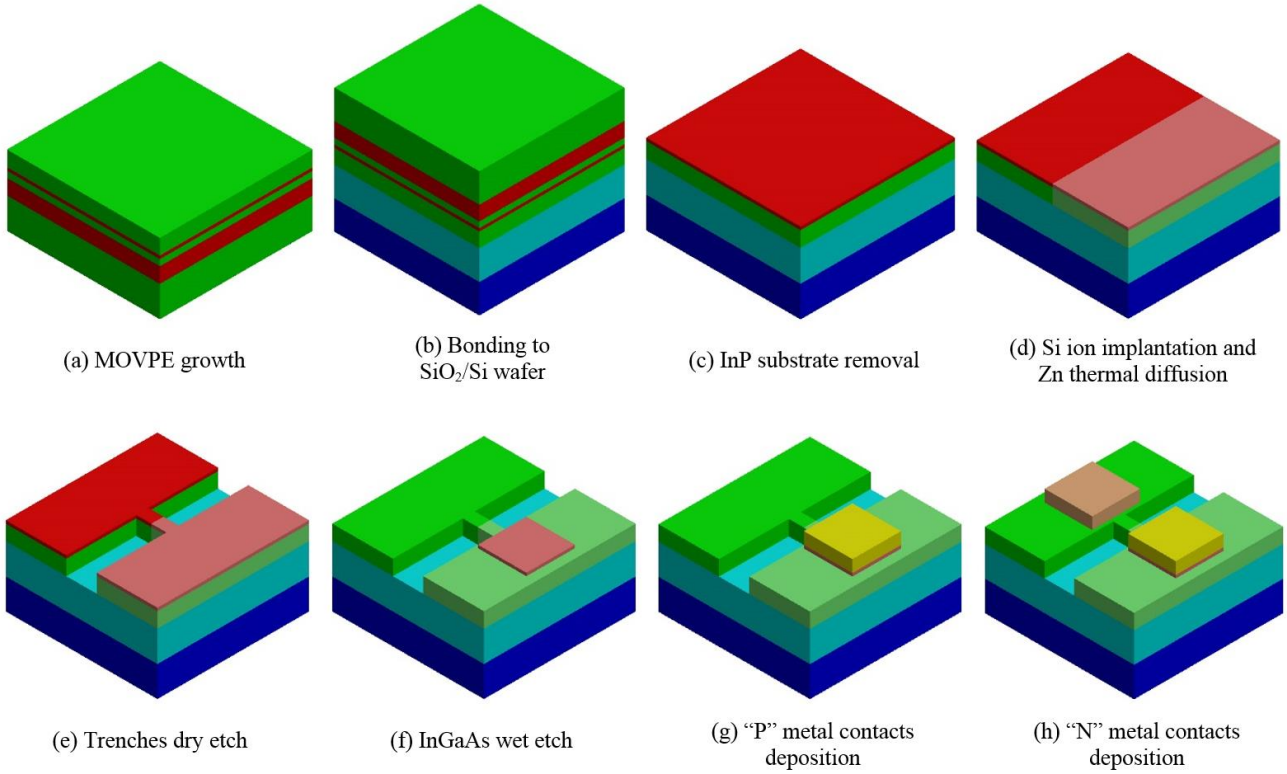

Figure 1. Schematic view of the fabrication process.

3. SI ION IMPLANTATION

Ion implantation is a robust way for selective doping of semiconductor layers as it gives the possibility of good control over doping profile and doping level. Several types of dopants can be used for n-type doping of InP: examples are Group IV (Si, Ge, Sn) and Group VI elements (S, Se, Te)[9]. The best results can be achieved using Si as it introduces the least amount of lattice damage and does not redistribute to a large extent during subsequent high temperature annealing. However, lattice damage introduced by Si ion implantation can still be significant[10,11], with the most damage located in the surface layer. For that reason, we perform Si ion implantation in the InGaAs/InP membrane with InGaAs on top, which is subsequently wet etched during the following processing.

To determine the important parameters of Si ion implantation, such as optimal energy of ions and minimal resist thickness, which is enough to block all Si^+ ions, simulation of Si ion implantation using Stopping Range of Ions in Matter (SRIM) software is carried out (Fig. 2). Optimal ion energy is found to be 180 keV and minimal resist thickness 700 nm. Dose is varied between $2 \cdot 10^{13}$ cm^{-2} and $2 \cdot 10^{14}$ cm^{-2}, which correspond to $6.7 \cdot 10^{17}$ cm^{-3} – $6.7 \cdot 10^{18}$ cm^{-3} Si concentration in InP. Sample tilt is 7° to prevent channeling effects, implantation is conducted at room temperature.

To be able to pattern structures for ion implantation with the size of critical dimension down to 300 nm, we use DUV lithography. Thickness of bottom anti-reflective coating (BARC) is fixed to be 65 nm, thickness of DUV resist is chosen to be 750 nm.

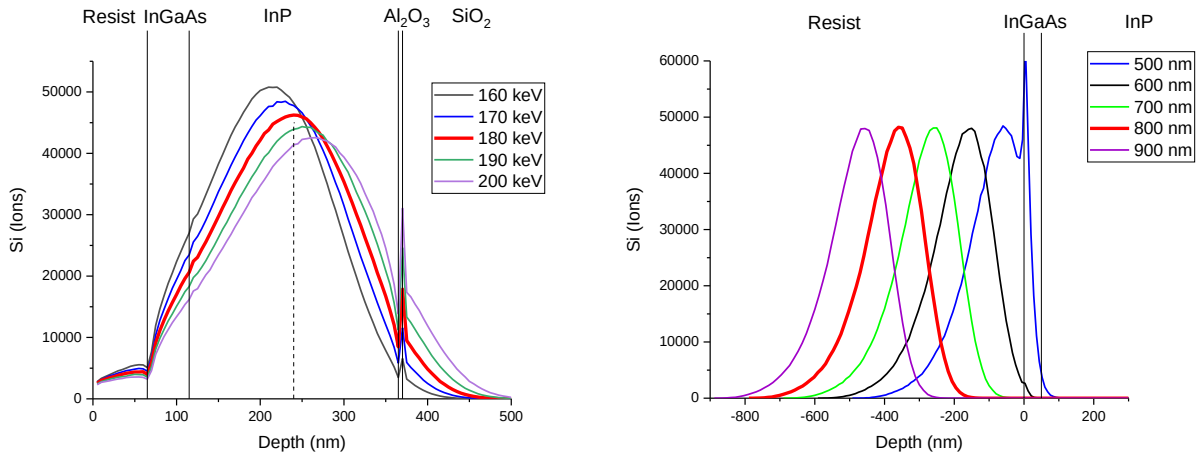

Figure 2. Results of Si ion implantation using SRIM software. Left: variation of Si ion energy. Right: variation of DUV resist thickness with fixed ion energy (180 keV).

After ion implantation Si impurities need to be electrically activated. Activation is done by rapid thermal annealing at 800°C for 30 s. Since InGaAs/InP can't withstand that high temperature, we need to protect it with deposition of a cap layer. SiN_x and SiO_2 cap layers turned out to be the bad choices: the InGaAs/InP membrane deteriorated a lot after annealing. Eventually, boron phosphorus silicate glass (BPSG) was found to be able to protect InGaAs/InP during annealing. We attribute that to BPSG's ability to reflow at high temperatures, which leads to reducing stress.

Electrical characterization of Si implanted n-InP is done by transmission line measurement (TLM) of specially designed test structures: "N" metal contacts with different distances between them. By measuring resistance between different pairs of contacts, we can get information about sheet resistance R_S and contact resistance R_C by extrapolating data with the formula

$$R = R_S \cdot \frac{L}{W} + 2R_C, \quad (1)$$

where R is resistance between two particular metal contacts, L is distance between contacts and W is width of n-InP between contacts (Fig. 3). R_S and R_C values are given in Table 1.

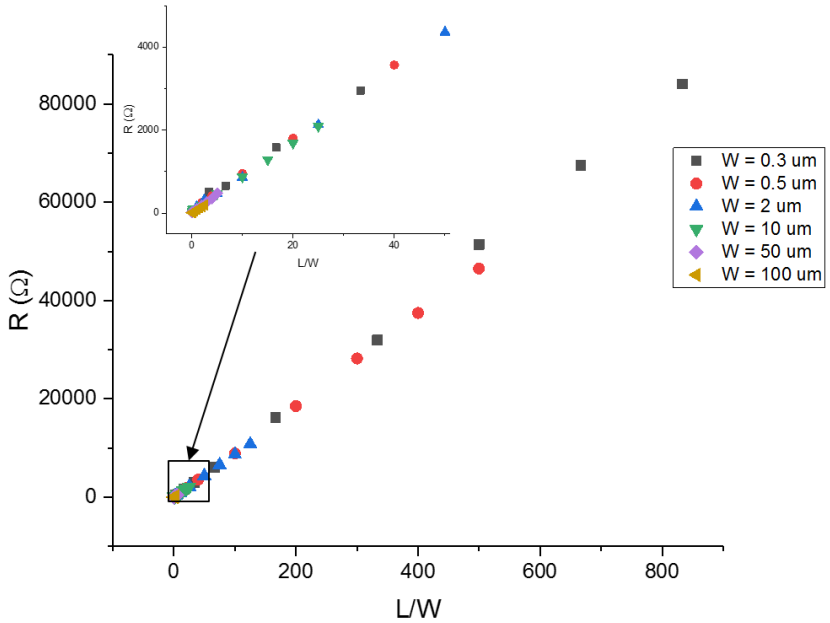

Figure 3. Transmission line measurement data for sample with $2 \cdot 10^{14}$ cm^{-2} implantation dose.

Hall effect measurements were conducted for n-InP using fabricated Hall bar structures in -2 — 2 T magnetic field range, values of Hall carrier concentration n_{Hall} and mobility μ_{Hall} are given in Table 1.

Table 1. Electrical properties of Si ion implanted n-InP membrane.

Total implantation dose, cm^{-2}	$2 \cdot 10^{13}$	$2 \cdot 10^{14}$
R_S, Ω□	328 ± 3	75 ± 1
R_C, Ω	12.9 ± 1.2	3.8 ± 0.3
n_{Hall}, cm^{-3}	$3.3 \cdot 10^{17}$	$2.9 \cdot 10^{18}$
Activation ratio, %	49	44
μ_{Hall}, $\frac{cm^2}{V \cdot s}$	2140	1040

In case of implantation dose $2 \cdot 10^{14}$ cm^{-2}, obtained carrier concentration is as high as $2.9 \cdot 10^{18}$ cm^{-3}, however, with the penalty of decreased carrier mobility (compared with the sample with lower dose). Nevertheless, these results are promising for application in p-i-n structures in InP membrane. Even if activation annealing temperature is decreased from 800°C to some lower value (to avoid possible deterioration of the active material e.g. quantum wells), n-InP resistance is expected to be usable.

4. ZN THERMAL DIFFUSION

Whereas ion implantation is an effective technique to create selective areas of n-type InP, for p-type InP it is hindered by low electrical activation ratios of p-type dopants. One alternative solution is to use Zn thermal diffusion in the MOVPE reactor with diethylzinc (DEZn) as Zn source[12,13,14]. This process takes place at 500-550°C under AsH_3 atmosphere with H_2 as a carrier gas. The diffusion is conducted in an Emcore Discovery D125 turbodisk system and in all the following experiments AsH_3 flow is 175 sccm. Overall gas flow is around 28000 sccm and chamber pressure is kept at 80 mbar. 100 nm of plasma enhanced chemical vapor deposited (PECVD) SiO_2 is used as a masking material. Before diffusion the sample is cleaned in concentrated sulfuric acid, followed by an annealing step at 650°C under AsH_3. After diffusion rapid thermal annealing at 450°C for 5 minutes under N_2 atmosphere is used to activate Zn dopants and clean sample from possible hydrogen-related impurities.

We started investigation of Zn diffusion with a test run on a 2" InP substrate with 50 nm of lattice-matched InGaAs on top without SiO_2 mask to be able to get information about carrier concentration profile by using an electrochemical capacitance-voltage (eCV) profiler. Diffusion was carried out at 505°C with molar flow ratio [DEZn] : [AsH_3] = 1 : 5.5 for 5 and 10 minutes. According to eCV measurements data (Fig. 4), hole concentration of ~10^{18} cm^{-3} in InP can be achieved for 250 nm top layer for durations larger than 10 minutes.

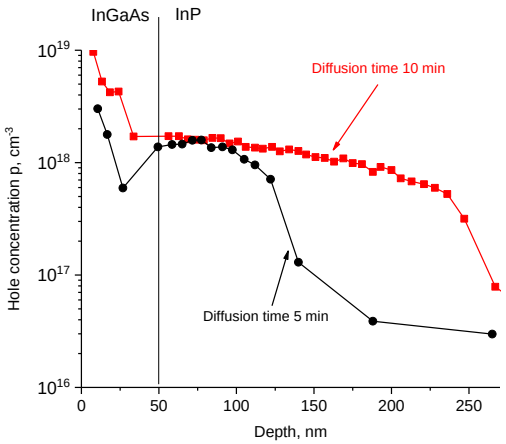

Figure 4. Hole concentration profiles in InGaAs/InP for different diffusion durations measured by eCV profiler.

For samples with an InGaAs/InP membrane bonded to SiO_2/Si, eCV profiling is difficult due to the thick dielectric SiO_2 layer. Transmission line measurements were carried out for the bonded InGaAs/InP/SiO_2/Si sample, which was Zn diffused with the parameters mentioned above (diffusion duration was 30 min). Surprisingly, sheet resistance of p-InP was found to be 3820 Ω□ (Fig. 5), which, assuming mobility 200 $cm^2/V/s$, corresponds to hole concentration being only $2.4 \cdot 10^{17}$ cm^{-3}, almost one order of magnitude lower than for InP substrate based sample. This can be attributed to difference in Zn diffusion mechanism in InGaAs/InP membrane on Si and InP substrates, or it might be equipment-related.

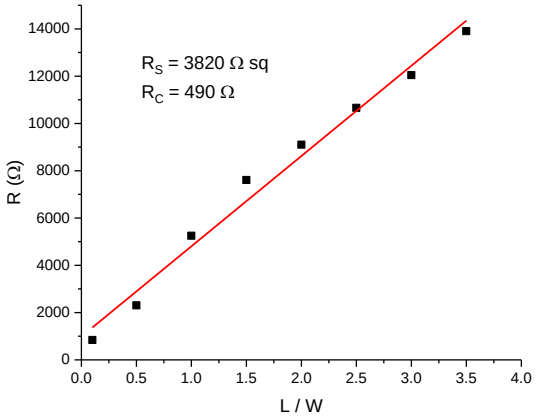

Figure 5. Transmission line measurements data for p-InP membrane on SiO_2/Si (Zn diffusion at 505°C, 30 min).

Higher diffusion temperature was tried (540°C), but it resulted in even less pronounced effect of Zn diffusion on not only the InP membrane, but also the InGaAs/InP membrane with InGaAs not being etched (remaining InGaAs would enhance possible effect of Zn diffusion). Estimated value of sheet resistance for p-InGaAs/InP was increased by one order of magnitude (Fig. 6).

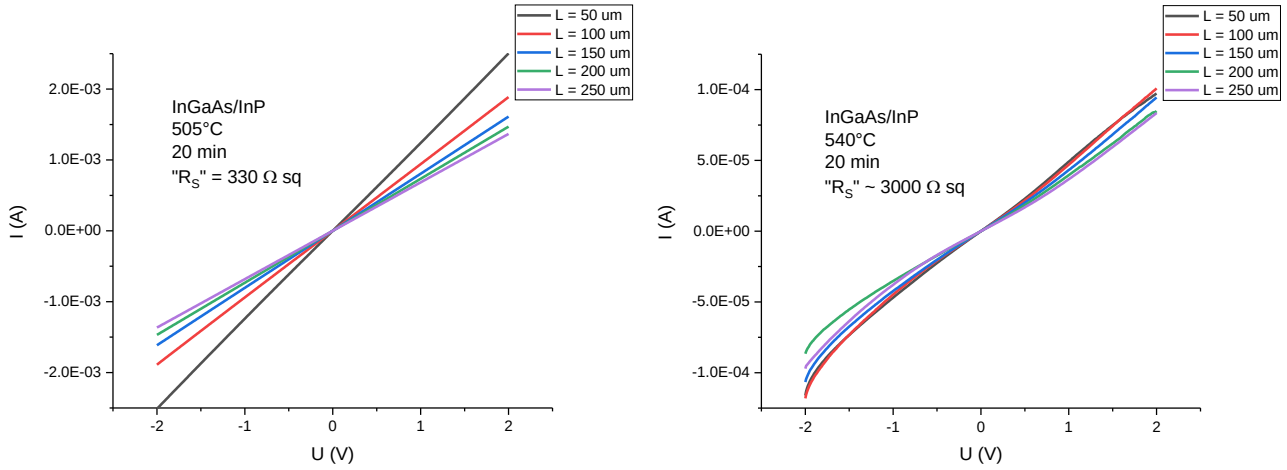

Figure 6. IV curves for p-InGaAs/InP membranes on SiO_2/Si. Left: Zn diffusion T = 505°C. Right: T = 540°C.

Eventually, DEZn molar flow was found to be of crucial importance for the zinc diffusion process. By adjusting different parameters, which have influence on DEZn molar flow, we achieved significant reduction in values of both p-InGaAs/InP and p-InP sheet resistances (Fig. 7).

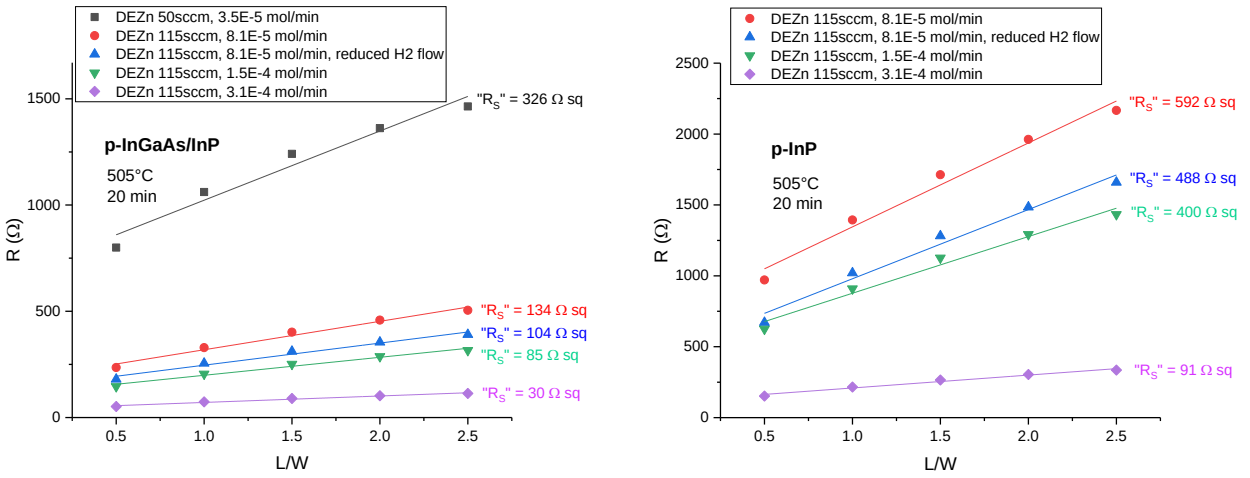

Figure 7. Transmission line measurements data for (left) p-InGaAs/InP and (right) p-InP membranes on SiO_2/Si for different DEZn molar flows during Zn diffusion. Note: actual sheet resistance values are expected to be several times larger due to not ideal TLM test structures for this batch of samples.

For DEZn molar flow $3.1 \cdot 10^{-4}$ mol/min (highest possible value using our DEZn bubbler), 505°C and diffusion duration of 20 minutes we obtained p-InP membrane with R_S being only 690 Ω□, which corresponds to hole concentration $1.3 \cdot 10^{18}$ cm^{-3} (Fig. 8).

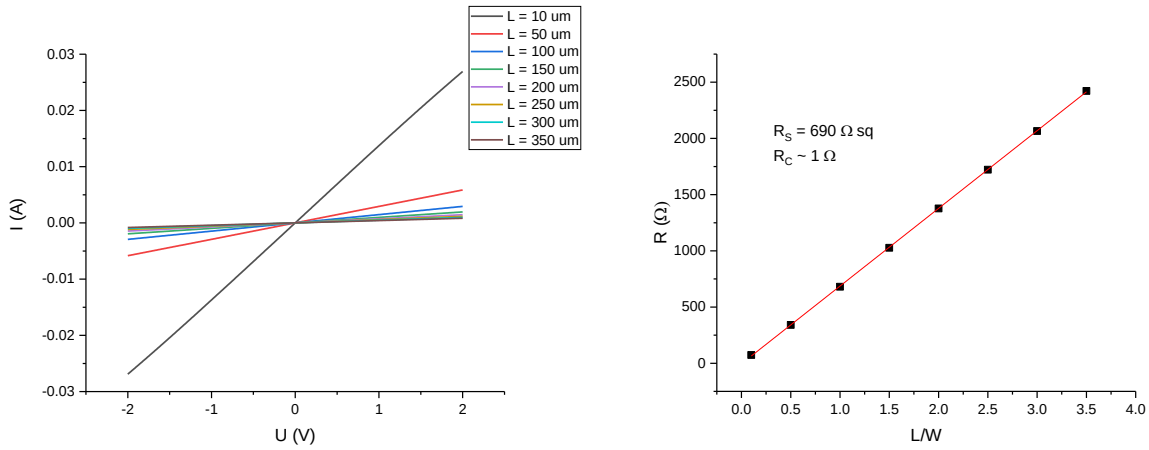

Figure 8. Left: IV curves for p-InP (Zn diffusion at 505°C, 20 minutes, DEZn molar flow $3.1 \cdot 10^{-4}$ mol/min). Right: transmission line measurements data for the same sample.

In some cases we observe deterioration of initially perfect InGaAs surface after Zn diffusion. This deterioration is non-uniform and somewhat random. The same SiO_2 mask openings can be deteriorated in quite different manner after Zn diffusion (Fig. 9). Moreover, this deterioration translates into underlying InP layer. Also there is a tendency of decrease in deterioration with increase of mask opening size, with smallest mask openings being most affected.

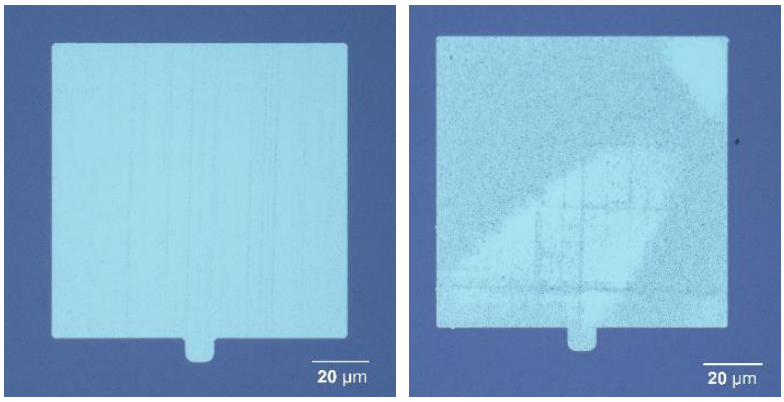

Figure 9. Optical microscope images of SiO_2 mask openings after Zn diffusion.

With closer view this deterioration looks like trenches, which are aligned in approximately the same direction, as seen on atomic force microscopy (AFM) pictures (Fig. 10).

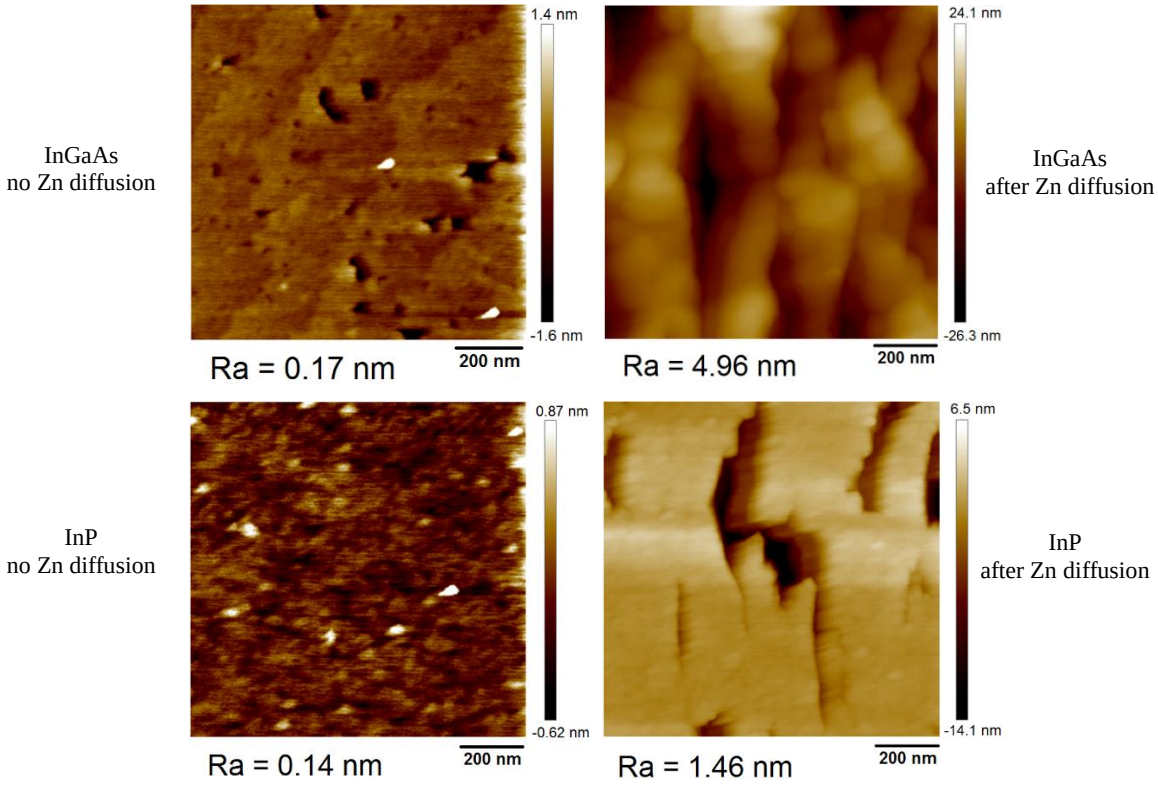

Figure 10. AFM images of InGaAs (top) and InP (bottom) surfaces without Zn diffusion (left) and after Zn diffusion (right).

No significant effect on electrical properties was observed due to deterioration of the surfaces. However, it could contribute to additional optical losses in the future device.

5. P-I-N JUNCTION

With use of abovementioned techniques for InP doping, it is possible to fabricate lateral p-i-n junction in InP membrane on SiO_2/Si substrate. An initial result can be seen on Fig. 11. Characteristic curve and light response indicate successful fabrication of p-i-n junction.

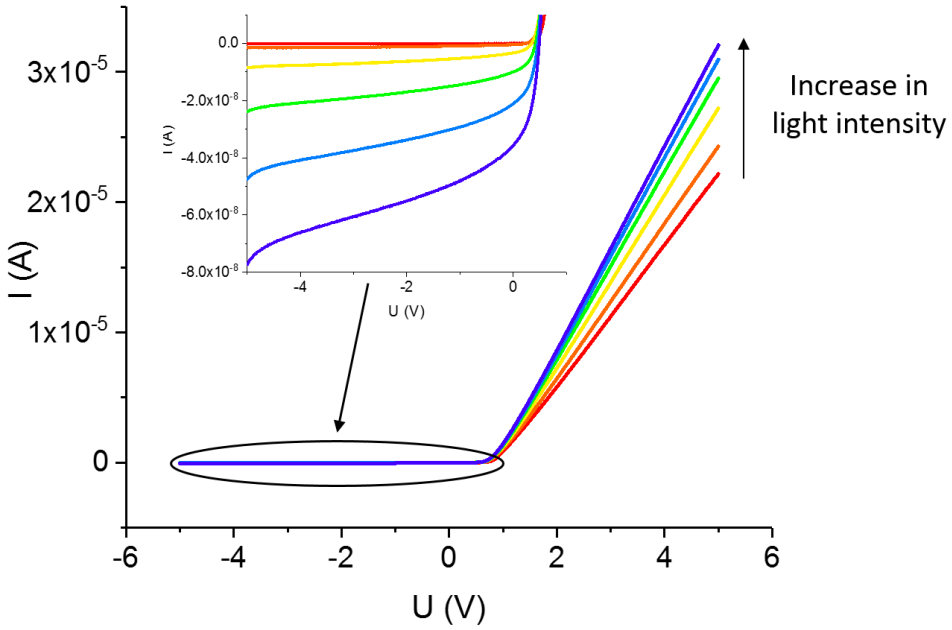

Figure 11. IV curves of p-i-n junction in InP membrane on SiO_2/Si substrate under different illumination levels.

6. CONCLUSION

We have investigated and optimized Zn thermal diffusion in MOVPE reactor and Si ion implantation as efficient methods to fabricate lateral p-i-n junction in InP membrane bonded to SiO_2/Si substrate. Carrier concentration levels of $1.3 \cdot 10^{18}$ cm^{-3} for p-InP and $2.9 \cdot 10^{18}$ cm^{-3} for n-InP are successfully demonstrated.

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